ME50N06A/ME50N06A-G

N- Channel 60V (D-S) MOSFET

GENERAL DESCRIPTION

The ME50N06A is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as LCD inverter, computer power management and DC to DC converter circuits which need low in-line power loss.

FEATURES

- $R_{DS(ON)} \leqq 22m\Omega @ V_{GS}=10V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

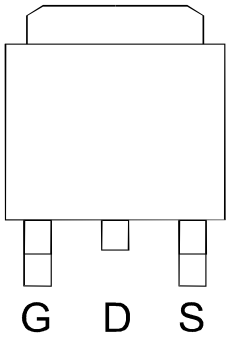
APPLICATIONS

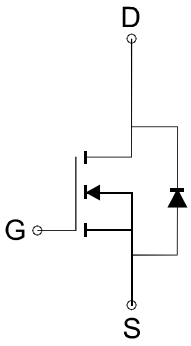
- Power Management
- DC/DC Converter
- LCD TV & Monitor Display inverter
- CCFL inverter
- Secondary Synchronous Rectification

PIN CONFIGURATION

(TO-252-3L)

Top View





N-Channel MOSFET

Ordering Information: ME50N06A (Pb-free)

ME50N06A-G (Green product-Halogen free)

Absolute Maximum Ratings (T_C=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C=25℃	I_D	35.1	A
	T_C=70℃		28.1	
Pulsed Drain Current		I_{DM}	140	A
Maximum Power Dissipation	T_C=25℃	P_D	59.5	W
	T_C=70℃		38.1	
Operating Junction Temperature		T_J	-55 to 150	℃
Thermal Resistance-Junction to Case*		$R_{\theta JC}$	2.1	℃/W

* Notes: The device mounted on 1in^2 FR4 board with 2 oz copper

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Electrical Characteristics (T_C =25℃ Unless Otherwise Specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	60			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	2		4	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=60V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance[a]	V_{GS}=10V, I_D= 50A		17	22	mΩ
V_{SD}	Diode Forward Voltage	I_S=50A, V_{GS}=0V		1.0	1.2	V
DYNAMIC						
Qg	Total Gate Charge	V_{DD}=48V, V_{GS}=10V, I_D=50A		37.1		nC
Qg	Total Gate Charge	V_{DD}=48V, V_{GS}=4.5V, I_D=50A		10.9		
Qgs	Gate-Source Charge			14.3		
Qgd	Gate-Drain Charge			8.3		
Ciss	Input capacitance	V_{DS}=15V, V_{GS}=0V, f=1MHz		2286		pF
Coss	Output Capacitance			172		
Crss	Reverse Transfer Capacitance			53		
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=30V, V_{GS}=10V, R_G=3.6Ω, R_L=30Ω I_D=1A		27.7		ns
t_r	Turn-On Rise Time			5.1		
$t_{d(off)}$	Turn-Off Delay Time			54.2		
t_f	Turn-Off Fall Time			5.5		

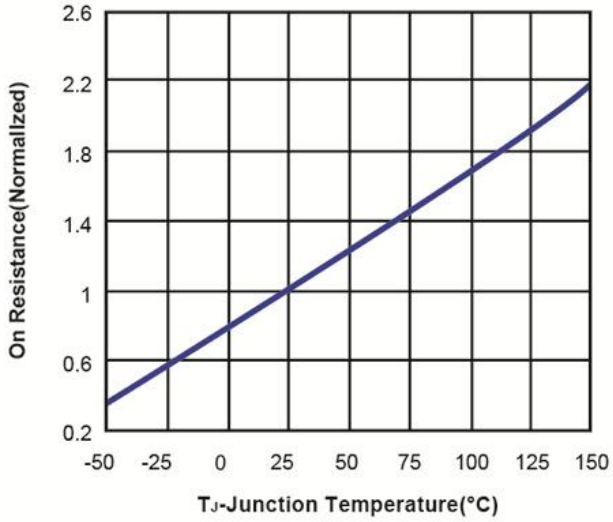
Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

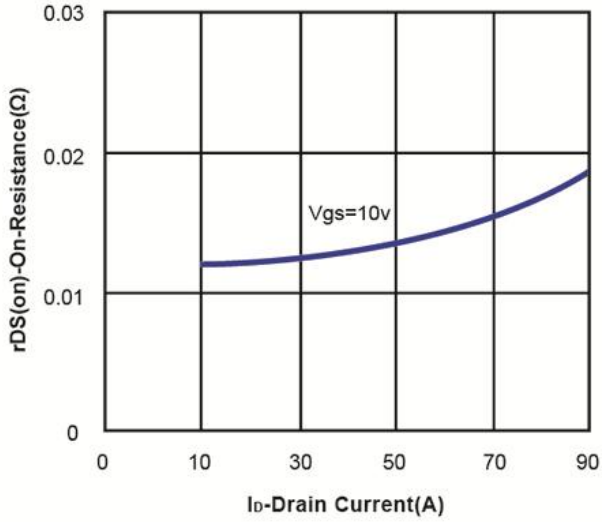
N- Channel 60V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted)

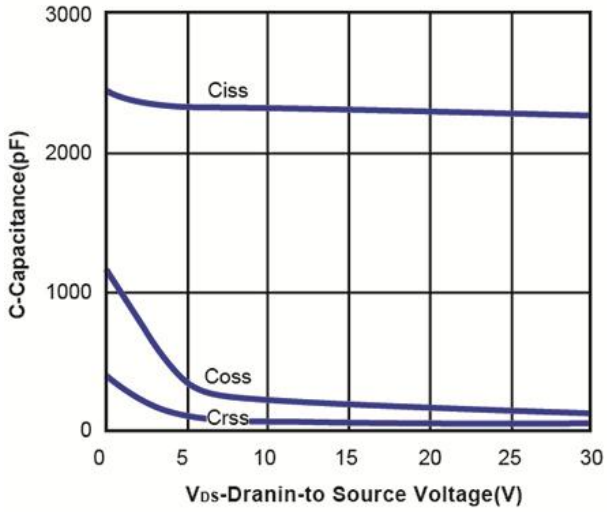
On Resistance vs. Junction Temperature



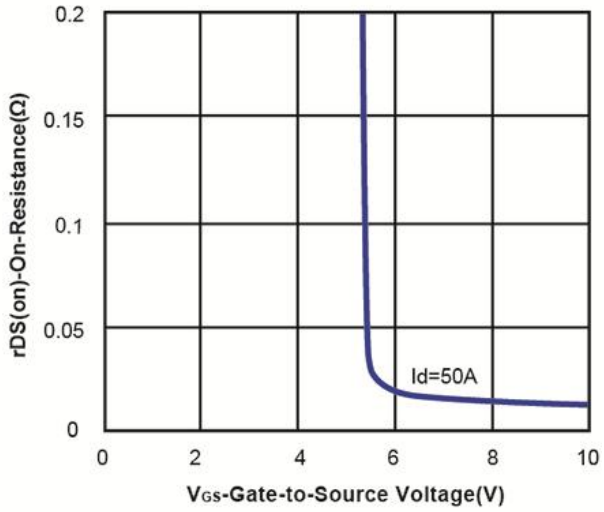
On Resistance vs. Drain Current



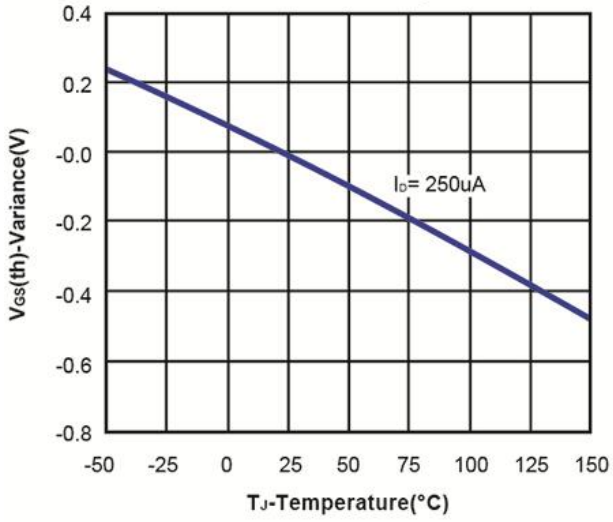
Capacitance



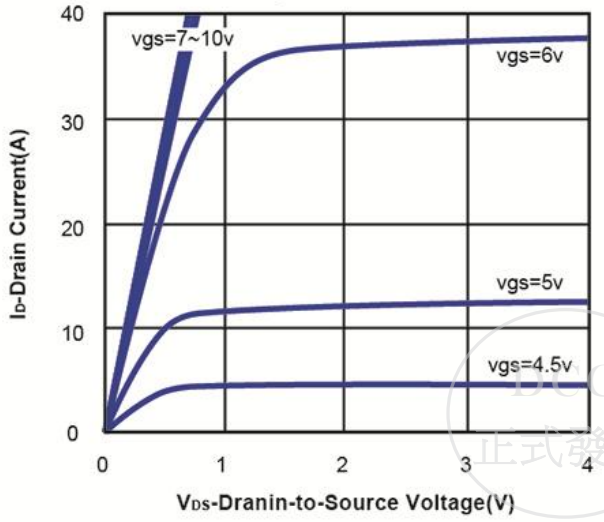
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage



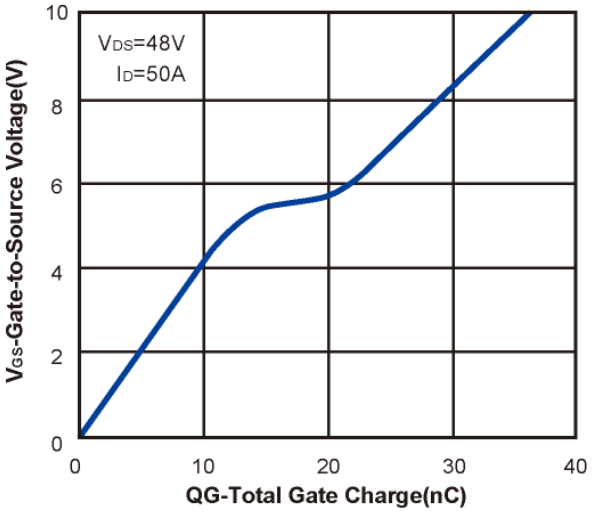
On-Region Characteristics



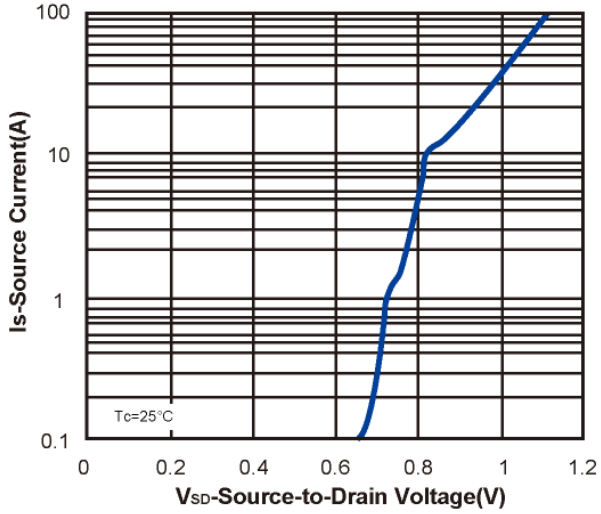
N- Channel 60V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted)

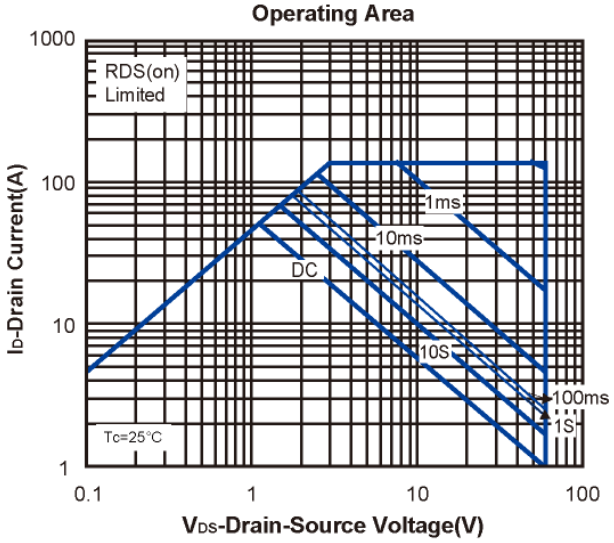
Gate Charge



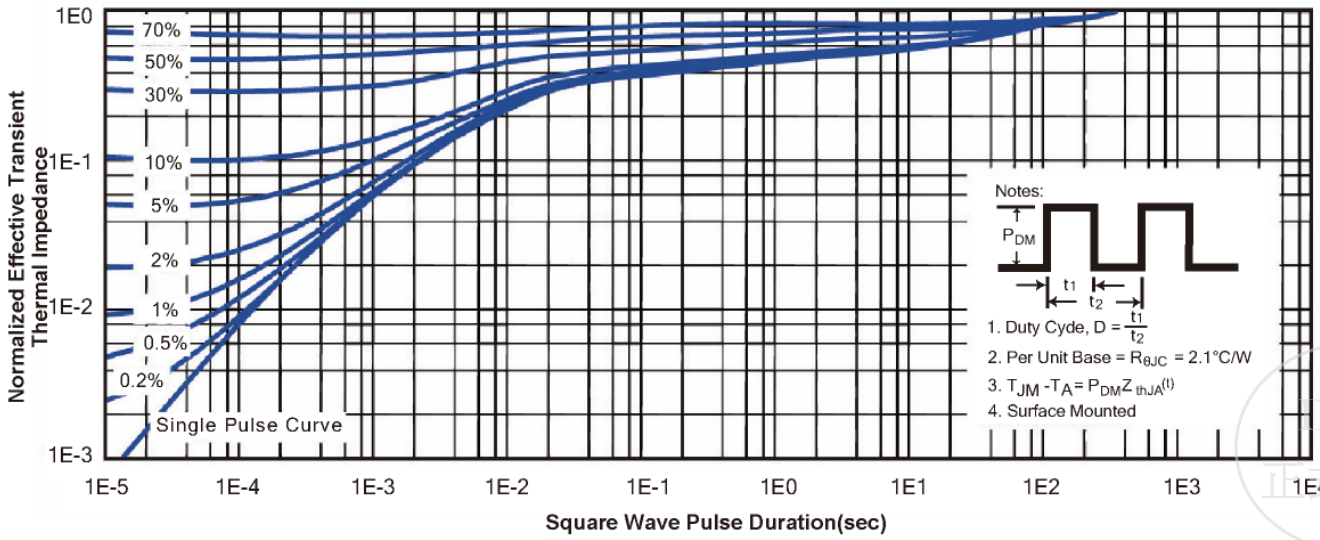
Body-diode characteristics



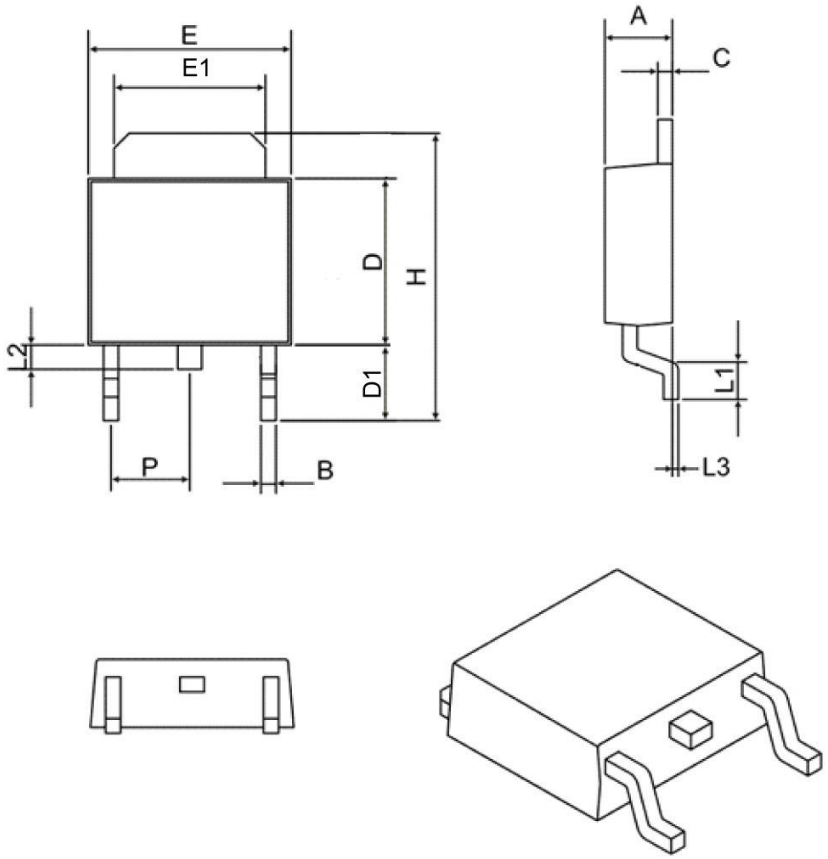
Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



TO-252-3L Package Outline



SYMBOL	MIN	MAX
A	2.10	2.50
B	0.40	0.90
C	0.40	0.90
D	5.30	6.30
D1	2.20	2.90
E	6.30	6.75
E1	4.80	5.50
L1	0.90	1.80
L2	0.50	1.10
L3	0.00	0.20
H	8.90	10.40
P	2.30 BSC	